UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/578,980	12/27/95	KAMAKURA T	39-5461-0

B5M1/0209

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON VA 22202

EXAMINER	
WILLE.D	
ART UNIT	**PAPER NUMBER**
2508	

DATE MAILED: 02/09/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/578,980	Applicant(s) Kamakura
	Examiner Douglas Wille	Group Art Unit 2508

☒ Responsive to communication(s) filed on *Dec 15, 1997* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-10* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-10* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Finality Withdrawn

1. Finality of the rejection of paper number 8 is withdrawn.

Claim Rejections - 35 USC § 112

2. Claims 8, 9, and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 8, 9, and 10 refer to a dense layer. This term is not defined and does not correspond to the usual meaning of dense. Calling a layer dense would appear to refer to the mass density but density, in general, could refer to such factors as electron density. These claims also refer to the lattice constant as being 10^{-2}. This is not understood since a lattice constant should have dimensions and second, it is in a range which is not physical, no matter what the dimensions. Typical lattice constants are in the range of several angstroms and for silicon, for instance, the lattice constant is 5.43 angstroms.

Claim Rejections - 35 USC § 102

4. Claims 1, 3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Scifres et al.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. With respect to claim 1, Scifres et al. describe a double hetero-structure LED (see Figure 2 and column 4, lines 13 - 30) with an AlGaAs clad layer 31, an undoped InGaAs active layer 29 and a second AlGaAs clad layer 25 which uses a strain layer 27 to prevent defect migration to the active region (column 1, line 44).

7. With respect to claim 3, the hetero-junction employs an undoped layer between two cladding layers.

8. With respect to claim 5, Scifres et al. discuss the use of a buffer layer (column 3, line 33).

Claim Rejections - 35 USC § 103

9. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scifres et al. in view of Inoue et al.

10. With respect to claim 2, Scifres et al. show the use of a strain layer to prevent defect migration and discuss the use of a buffer layer (column 3, line 33), which is known to also limit defect migration and also discuss adding other strain layers (column 4, line 64). Inoue et al. discuss (see abstract) the use of multiple defect regions to limit defect migration and it would have been obvious to include a second strain layer as taught by Inoue et al. to supplement the buffer region.

11. With respect to claim 8, Scifres et al. discuss the basic device structure and refer to the strain layer thickness as being approximately 10 nm (column 4, line 47). Scifres et al. also discusses the lattice mismatch as being less than or equal to 4% (column 4, line 49). Inoue et al. discusses the defect density as being in the range of 10^6 /cm^2 which corresponds to a value greater than 10^4 /cm^3. It would have been obvious to provide the Scifres et al device with the defect density taught by Inoue et al. to improve the defect protection.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scifres et al. in view of Sugawara et al.

13. Scifres et al. describe a double hetero-structure LED. Sugawara et al. discuss an LED structure which specifically calls out a current spreading layer 15 (cover Figure) and detail the use of a buffer layer 32 (Figure 6). It would have been obvious to include the current spreading layer and the buffer layer to provide a more uniform output with improved reliability.

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scifres et al. in view of Sugawara et al.

15. Scifres et al describe a double hetero-junction LED with clad layers enclosing an undoped region and having a strain layer to prevent defect migration. Sugawara et al. provide details of a buffer layer 32 (Figure 6), a current spreading layer 15 (cover Figure) and a reflective layer 33 (Figure 6). It would have been obvious to one skilled in the art at the time of the invention to include the current spreading layer, the buffer layer, and the reflective layers to improve device reliability and performance.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scifres et al. in view of Sugawara et al. and further in view of Inoue et al.

17. Scifres et al. describe a double hetero-junction LED with clad layers enclosing an undoped region and having a strain layer to prevent defect migration. Sugawara et al. provide details of a buffer layer 32 (Figure 6), a current spreading layer 15 (cover Figure) and a reflective layer 33 (Figure 6). Scifres et al. discusses the strain layer thickness as being approximately 10 nm (column 4, line 47). Scifres et al. also discusses the lattice mismatch as being less than or equal to 4% (column 4, line 49). Inoue et al. discusses the defect density as being in the range of 10^6 /cm^2 which corresponds to a value greater than 10^4 /cm^3.

18. Claims 5, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scifres et al. in view of Sugawara et al. and further in view of Inoue et al.

19. With respect to claim 7, Scifres et al. describe a double hetero-junction LED with clad layers enclosing an undoped region and having a strain layer to prevent defect migration. Sugawara et al. provide details of a buffer region, a current spreading region and a reflective layer. Inoue et al. describe the use of multiple defect controlling layers. It would have been obvious to modify the Scifres et al. device to include the current spreading layer, the details of the buffer layer, the reflective layers and a second layer as taught by Sugawara et al. and Inoue et al. to prevent defect migration and enhance the device output.

20. With respect to claim 5, Sugawara et al. describe the buffer layer as helping prevent defect migration (column 9, line 53).

21. With respect to claim 10, Scifres et al. discuss the strain layer thickness as being approximately 10 nm (column 4, line 47). Scifres et al. also discuss the lattice mismatch as being less than or equal to 4% (column 4, line 49). Inoue et al. discuss the defect density as being in the range of 10^6 /cm^2 which corresponds to a value greater than 10^4 /cm^3.

Conclusions

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A. Wille whose telephone number is (703) 308-4949.

23. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose number is (703) 308-0956.

Sara W Crane
SARA W. CRANE
PRIMARY EXAMINER
GROUP 2500

DAW Dww

February 4, 1998

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER